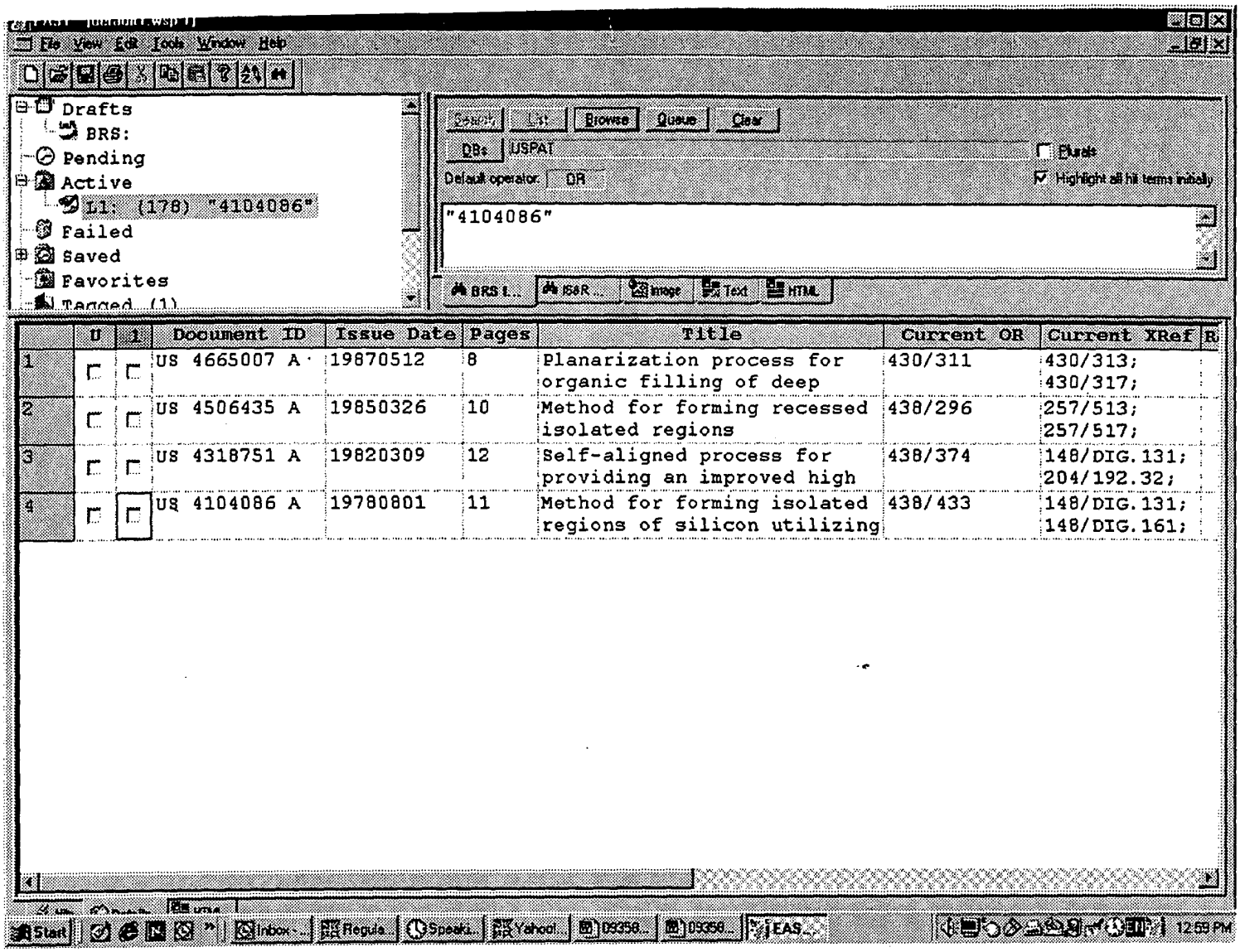

	U	1	Document ID	Issue Date	Pages	Title	Current OR	Current XRef	R
1	☐	☐	US 4665007 A	19870512	8	Planarization process for organic filling of deep	430/311	430/313; 430/317;	
2	☐	☐	US 4506435 A	19850326	10	Method for forming recessed isolated regions	438/296	257/513; 257/517;	
3	☐	☐	US 4318751 A	19820309	12	Self-aligned process for providing an improved high	438/374	148/DIG.131; 204/192.32;	
4	☐	☐	US 4104086 A	19780801	11	Method for forming isolated regions of silicon utilizing	438/433	148/DIG.131; 148/DIG.161;	

details in accordance with practical manufacturing steps.

FIGS. 26A to 26G show the manufacturing steps. First, two Si substrates 1 and 4 are prepared. One surface of each of Si substrates is mirror-polished. One substrate, i.e., Si substrate (first semiconductor substrate) 4 is a p^--type substrate for element formation, and has a resistivity of 70 to 100 Ω·cm. After p^+-type layer 6*a* is formed in the mirror-polished surface of substrate 4 by diffusing boron at a high concentration SiO_2 film 3*a* having a thickness of about 1 μm is formed on the surface of the resultant structure (FIG. 26A). The other substrate, i.e., Si substrate (second semiconductor substrate) 1 may be of p- or n type, and has no limitation as to specific resistivity. Such two substrates 1 and 4 are bonded to each other by a silicon wafer direct-bonding technique. Then, a surface of substrate 4, which is opposite to the bonding surface, is polished to obtain p^--type Si layer 4 having a thickness of about 60 μm (FIG. 26B). SiO_2 film 3*a* is used for element isolation. It has been confirmed from experiments performed by the present inventors that in order to reduce warpage of the resultant wafer, SiO_2 film 3*a* must be formed on element formation substrate 4 in advance, and that bonding interface 2 must face the upper surface of SiO_2 film 3*a* which is formed on element formation substrate 4 in advance.

The steps of practical direct bonding are performed in the following manner. Substrates to be bonded are cleaned by an H_2SO_4—H_2O_2 mixture solution, HCl—H_2O_2 mixture solution, aqua regia, or the like. Subsequently, the substrates are cleaned by water for about ten minutes, and are dried by a spin dryer or the like. The substrates subjected to these processes are set in a clean atmosphere below, e.g., class 100, and their mirror-polished surfaces are bonded to each other in a state wherein substantially no contaminant is present therebetween. With this process, the two substrates are bonded to each other with a certain strength. When the substrates bonded to each other in this manner are subjected to heat-treatment in a diffusion furnace or the like, bonding strength is increased, and the two substrates are completely bonded. An increase in bonding strength is observed at about 200° C. or more, preferably at 800° to 1200° C. No special attention need be paid to the atmosphere for the heat-treatment process. For example, heat-treatment can be performed in an oxygen, nitrogen, hydrogen, inert gas, steam, or a gas mixture thereof. In the embodiment, cleaning was performed by an H_2SO_4—H_2O_2 mixture solution and an HCl—H_2O_2 mixture solution, and heat-treatment was performed a nitrogen atmosphere including a small amount of oxygen at 1,100° C. for two hours.

Subsequently, the surface of Si substrate 4 is lapped and polished to reduce the thickness. And, SiO_2 film 31 is formed on the upper surface of Si substrate 4. Tapered isolation trench 32 is then formed by etching, e.g., anisotropic etching Si layer 4 to a depth reaching SiO2 film 3*a* using pattern 31*a* obtained by patterning SiO2 film 31 as a mask. With this process, Si layers 4*a* and 4*b* are isolated in the forms of islands (FIG. 26C). Boron is diffused in isolation trench 32 by diffusion so as to form p^+-type layers 6*b* in the side walls of island Si layers 4*a* and 4*b*. P^+-type layers 6*b* are integrated with p^+-type layer 6*a* on the bottom of the isolation trench so as to constitute p^+-type layer 6. SiO_2 film 3*b* is formed in the side wall of each Si layer 4 by another thermal oxidation of the side wall. Then, SiO_2 film 31 on the surface of Si layer 4*b* on the low breakdown voltage element side is patterned to form pattern 31*a*. Si layer 4 is etched by using pattern 31*a* as an etching mask to form recesses in the element region. Phosphorus or antimony is introduced in the recesses at a high concentration by diffusion to form n^+-type layers 21*a* and 21*b* (FIG. 26D).

Subsequently, SiO_2 film 31*b* on the surface of Si layer 4*b* in which the recesses are formed is removed, and epitaxial growth of Si is performed to form high-resistance n^--type layer 22. At the same time, polysilicon layer 5 is formed on SiO_2 film 31*a* on the isolation region covered with SiO_2 film 3*b* and on the other Si layer, i.e., layer 4*a* (FIG. 26E). In this case, there a thin polycrystalline silicon layer is formed on the oxide film 3*b*, a simultaneous growth of the epitaxial layer 22 and the polycrystralline silicons layer 22 can be formed more easily. The growth layer surface is then lapped and polished so that the thickness of substrate 4 is 20 to 100 μm, and n^--type layers 22*a* and 22*b* are buried in the recesses to obtain a flat state wherein polysilicon film 5 is buried in the isolation trench (FIG. 26F). Since n^--type layer 22 is buried only in the recesses and other portions thereof are removed, only portions of SiO_2 film 31*b* overhanging in the recesses need be theoretically removed when the epitaxial growth process in FIG. 26E is performed. However, if crystal growth is performed while SiO_2 film 31*b* is locally left, a high-quality single crystal cannot be buried, and hence defects are often caused. In order to decrease the defects, SiO_2 film 31*b* on the surface of Si layer 4*b* is preferably removed substantially entirely in crystal growth, as described above.

Pnp transistor T2 and npn transistor T3 which are isolated from each other by a pn junction isolation are respectively formed in n^--type layers 22*a* and 22*b* buried in this manner.

More specifically, p-type layers 23 and 24 are formed in the surface region of n^--type 22*a* at a predetermined interval. Thereafter, collector, emitter, and base electrodes 27*a*, 28*a*, and 29*a* are formed. As a result, lateral type pnp transistor T2 having n^--type layer 22*a* serving as a base, and p-type layers 23 and 24 respectively serving as a collector and a emitter is formed.

p-type layer 25 is formed in the surface region of n-type layer 22*b* by impurity diffusion. In addition, n-type layer 26 is formed in the surface region of p-type layer 25. Then, collector, emitter, and base electrodes 27*b*, 28*b*, and 29*b* are formed to form vertical type npn transistor T3 having n^--type layer 22*b* as a collector, p-type layer 26 as a base, and n-type layer 26 as an emitter.

Subsequently, in p^--type Si layer 4*a*, p-type base layer 7 is formed in its peripheral portion, n-type source layer 8 is formed therein, n-type base layer 9 is formed in its central portion, and p-type drain layer 11 is formed therein by impurity diffusion. N^--type layer 10 serving as a guard ring is formed around n-type base layer 11 by impurity diffusion. Gate electrode 13 is formed on a region between n-type source layer 8 and n^--type layer 10 with gate insulating film 12 interposed therebetween. Then, drain electrode 15 is formed on p-type drain layer 11, and source electrode 14 is formed on n-type source layer 8 and p-type base layer 7 so as to be simultaneously in contact with layers 8 and 7, thereby obtaining IGBT-T1 (FIG. 26G).

In the semiconductor device obtained in the above-described manner, high breakdown voltage IGBT-T1 processing a large current can be electrically isolated